Bringing Design Technology and Architecture Closer Together: What Open Source Might Enable

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Open Source Design Technology
Design Crises: Cost, Expertise, Unpredictability

- Design cost: not scaling
- Design, process roadmaps not coupled
- Figure: Andreas Olofsson, DARPA, ISPD-2018 keynote

- Quality: also not scaling
- Design Capability Gap
- Available density: 2x/node
- Realizable density: 1.6x/node
- Figure: UCSD / 2013 ITRS
Design is Too Difficult!

- Tools and flows have steadily increased in complexity
  - Modern “Place and Route” tool: 10000+ commands/options

- Hard to design with latest tools in latest technologies
  - Even harder to predict design quality, schedule
  - Expert users are required
  - Increased cost and risk are not good for industry!

- Still have “CAD” mindset more than “DA” mindset
  - Again: assumes expert users

How do we escape this “local minimum”? 
U.S. DARPA IDEA: No-Humans, 24-Hours

IDEA will create a no-human-in-the-loop hardware compiler for translating source code to layouts of System-On-Chips, System-In-Packages, and Printed Circuit Boards in less than 24 hours

A. Olofsson, DARPA ISPD-2018 keynote

• Part of DARPA Electronics Resurgence Initiative
• Traditional EDA focus: ultimate quality
• New IDEA focus: ultimate ease of use
• No human in the loop, 24-hour turnaround time
  = “design-based equivalent scaling”
• Overarching goal: designer access to silicon
OpenROAD’s Foundation Technologies

24 hours, no humans – no PPA loss

Mindsets

- Achieve **predictability** from the user’s viewpoint
- Use cloud/parallel to recover solution **quality**
- Focus on reducing **time and effort = schedule, cost**

“**The Last Scaling Levers**: Quality, Schedule, Cost

- Quality
- Schedule
- Cost
The OpenROAD Project

- Initial target: digital IC flow “RTL to GDS”
  - Inputs: .v, .sdc, .lib, .lef
  - .def, .spef in point tools
  - config files, pre-characterizations required
  - Outputs: routed .def, timing/power reports

- Open source
- No-human-in-loop
  - Limited “knobs”, restricted field of use
  - Replace intelligent humans (partition, floorplan, …)

- Alpha release: July 2019
- v1.0 release: June 2020

See: https://theopenroadproject.org/publications/
https://github.com/The-OpenROAD-Project
Why Open Source? (details from DAC-2019 panel)

- Clarity
  - Leading edge becomes visible and well-defined
  - *Today*: EDA license terms include “no benchmarking”

- Better science
  - Advances are verifiable: no more “irreproducible results”
  - *Today*: Scientific research in EDA is constrained to be irreproducible!
    - E.g., cannot publish the Tcl scripts for commercial EDA tools that my students use

- Avoid reinventing wheels
  - Field advances more rapidly
  - *Today*: Students waste months trying to reconstruct papers
  - *Today*: Students waste months reimplementing basic algorithms, engines
OpenROAD Outreach: Workshops, Contests…

Open Source Community Contribution Awards (Nominations Open)

DAC'19 Birds of a Feather

WOSET 2019

ICCAD-2019 Contest C co-sponsorship

DAC'18 Birds of a Feather

WOSET 2018

EDA Futures Workshop
Open-Source EDA Isn’t New

• From Berkeley/MIT tools to The Bookshelf to …

DATC RDF Flow

- IEEE CEDA Design Automation Technical Committee
- Construct an academic reference design flow based on contest results for facilitating EDA research
- Run the flow from logic synthesis to detailed routing, and create final detailed-routed DEF
- Link to 2019 ISPD detailed routing contest and extend to cloud

Iris Jiang, DAC-2019 Open-Source Academic EDA Tools “Birds-of-a-Feather” meeting (wiki)
Open-Source EDA Tools Census

Adapted from Prof. Tsung-Wei Huang, DAC-2019 Session 37 talk

IDEA/POSH program launched

New Release  Total

66  7  8  9  10  12  13  16  18  23  24  25  29  31  32  34  36  37  39  43  49  57  81  91

New Release
Total

0  10  20  30  40  50  60  70  80  90  100

Adapted from Prof. Tsung-Wei Huang, DAC-2019 Session 37 talk
Tool Demographics

- Digital: 81%
- FPGA: 4%
- Analog: 13%
- Digital / Analog: 2%

Adapted from Prof. Tsung-Wei Huang, DAC-2019 Session 37 talk
Warning: 40 Years of Industry Learning Curve

• Commercial EDA has gone up a learning curve regarding how to architect the complex interactions between tools in the Synthesis, Place and Route tool chain

• 1980’s - focus was on point tools connected by files

• 1990’s – pervasive timing driven steps required tight connection to timing

• 2000’s – tightly coupled algorithms on a shared incremental substrate

• 2010’s – Advanced node effects, parallel processing, hyper-optimization
Incremental EDA Architecture: Shared Netlist

A. B. Kahng, 190623 ISCA Visioning

Tom Spyrou, DAC-2019 Open-Source Academic EDA Tools “Birds-of-a-Feather” meeting (wiki)
Warning: 40 Years of Industry Learning Curve

- Commercial EDA has gone up a learning curve regarding how to architect the complex interactions between tools in the Synthesis, Place and Route tool chain.
- 1980’s - focus was on point tools connected by files.
- 1990’s – pervasive timing driven steps required tight connection to timing.
- 2000’s – tightly coupled algorithms on a shared incremental substrate.
- 2010’s – Advanced node effects, parallel processing, hyper-optimization.
- OpenROAD Alpha will be a “1980’s” file-based flow.
- OpenROAD v1.0 production release targets a “2000’s” tightly coupled shared incremental architecture similar to commercial production tools.
  - Implies a first-ever shared DB layer in permissive open source...
Bringing Architecture Closer
Food for Thought: Our Two Worlds …

• “EDA / IC design world”
  • System-on-chip engineering teams have 1000s of headcount
  • Driving commercial EDA tools is difficult, w/huge PPA swings
  • New technology node can bring very modest PPA wins (note: pick one or two only)
    • Hard to know value of (device, material, integration) technology in advance
  • EDA VP R&D: 0.5% clock power reduction would be a home run in a competitive benchmark

• “Architecture world”
  • 40%, 25x, etc. improvements are frequently achieved
  • A recent draft on multi-die system integration: 50% iso-cost performance improvement, 30% iso-performance cost improvement

• How is this possible?
How to Estimate… \((\text{power, reliability, \ldots})\)?

- Tech files, signoff criteria, corners
- AVS
- Slack
- P&R + Optimization
- Timing/Noise
- Sim Results (Dyn.) Activity Factor (Static)
- IR Drop Map
- Timing / Glitches
- Power Analysis
- Power Trace
- Thermal Analysis
- Temp Map
- MTTF & Aging
- Task Mapping/Migration/(DVFS)
- Reliability Report
- Function  I Sim
- Sim vectors Benchmark RTL
(across analysis loops, scales, layers, …)?

Design, EDA

- P&R + Optimization
- Timing/Noise
- Slack
- AVS

Tech files, signoff criteria, corners

STA-IR loop
- Timing / Glitches
- IR Drop Map

Workload-Thermal loop
- Power Trace
- Temp Map
- Task Mapping/Migration/Rev

STA-Thermal loop
- Reliability Report

STA-Reliability loop
- MTTF & Aging

Power Analysis

Sim Results
(Static)

Architecture

Sim vectors
Benchmark RTL

Architecture
Not an Architect, Just a Fan…

- **ORION 2.0/3.0:**
  - Network on Chip Power and Area Model
    - ORION 2.0 ([download](download))
    - ORION 3.0 ([website](website))
- **CACTI-IO:**
  - Power, Area and Timing Models for The IO and PHY of Off-Chip Memory Interfaces ([report](report))
- **CACTI 7:**
  - New Tools for Interconnect Exploration in Innovative Off-Chip Memories ([website](website))
- **ITRS System Drivers, System Integration roadmaps**
- **Collaborations with architects**
  - …
Closer: Design-Tech Co-Optimization (DTCO)

**Design Technology**

- Architecture Design
- High Level Synthesis
- RTL
- Logic Synthesis
- Gate Netlist
- Extraction, Timing, Physical Verification
- Reading
- GDSII
- Manufacturing

**Manufacturing Technology**

- Design-Aware Manufacturing
- Manufacturing-Aware Design
- Performance & Power Benefit
- GAAFET
- Planar FET
- FinFET

**Design for Manufacturability (DFM)**

**Key Design Types**

- RV12 RISC-V
- GPU Core

**Key IPs/ Components**

- NAND2
- 6T SRAM
- D Flip-Flop

A. B. Kahng, 190623 ISCA Visioning
Closer: DTCO $\rightarrow$ Pathfinding

Applications, Markets

Internet Wave
Internet Boom, Cell Phone

Digital Wave
PC

Analog Wave
TV, VCR

Portability & Connectivity Wave
Wireless device

IoT/Edge and Cloud?
DL?
Vision/ ADAS?
VR/AR/MR?

Systems
Quantum Processor
Package On Package  D2W

D2D  Monolithic
Neuromorphic computing

Design Technology

Manufacturing Technology

Design for Manufacturing (DFM)

Design-Aware Manufacturing

Manufacturing-Aware Design

Key Design Type

RV12 RISC-V  GPU Core

Key IPs/ Components

NAND2, 6T SRAM, D Flip-Flop

Loop back is missing!!!
What “Together” Might Enable
Perhaps …

• … ML-powered, self-driving EDA tools and flows?
  • Restores access to hardware implementation!
  • Starts with collaborative generation of data
  • Unlocked by \{designs\} + \{tools\} + \{technology\}
    = Architects/designers + EDA researchers

• … Better oracles and constructive proofs of achievable PPAC (= DSE) at the absolute limits of a given technology and enablement?
  • “40%” or “25x” can be more rigorously supported
  • Maybe 50% or 35x could have been found!
  • Unlocked by ML in and around (open-source?) IC design tools and flows

• … What else?
Summary

Bringing Design Technology and Architecture Closer Together: What Open Source Might Enable

Open-Source Design Technology  
+ Bringing Architecture Closer  
+ What “Together” Might Enable  

= Food for Thought! 😊
THANK YOU!

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A few links:
- Presentations linked under News at [https://vlsicad.ucsd.edu/](https://vlsicad.ucsd.edu/)
- [https://theopenroadproject.org/](https://theopenroadproject.org/) and [https://theopenroadproject.org/outreach/](https://theopenroadproject.org/outreach/)
- [https://github.com/The-OpenROAD-Project/](https://github.com/The-OpenROAD-Project/)
- Machine learning “in and around IC design tools”:
  - [https://vlsicad.ucsd.edu/Publications/Conferences/356/c356.pdf](https://vlsicad.ucsd.edu/Publications/Conferences/356/c356.pdf)
  - [https://vlsicad.ucsd.edu/Publications/Conferences/360/c360.pdf](https://vlsicad.ucsd.edu/Publications/Conferences/360/c360.pdf)
  - Etc.