Building a Sustainable Open Source Hardware Ecosystem

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Google, CHIPS Alliance
Organic demand is growing...

Data is growing at a faster exponential than original Moore’s law
Growing demand

Trillions of searchers per year, >130T web addresses; indexed pages from over 165M domains; 200B links within apps indexed; 15% of searches we see every day are new. The knowledge graph maps out how more than 1 billion things in the real world are connected and over 70 billion facts about them.

The assistant is now available on more than 400 million devices; >one Google Home per second since October 2017. When Google began, we rolled out a new index about every month. Today, we generally index popular content from news sites and blogs within seconds or minutes of publication.

E.g. Search Features

- Web Search & Serve
- + more meaning extraction
- + multiple data repositories
- + complex I/O moves
- + cross-correlations

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Changing demand

Once maps were simple

Context: Social, Collaborative filtering, Personalization

Static rich media, Synthetic data, real-time

Google Cloud

+Instant search, live translate, knowledge graph, google now...
Finding new value in data: growing demand
Moore’s Law Slowing Down

Design Cost Skyrocketing

Original data collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten, dotted line extrapolations by C. Moore

Source: IBS
Google Makes Chips

Tensor Processing Unit

Cloud TPU

TPUv3
Promise of Open Source Hardware

The vision is of a collaborative ecosystem of reusable IP and tools.

- Quickly build common domain-agnostic parts
- Focus on innovation
- Build on the computer architecture *renaissance* due to EoML
Long History of Openness at Google

10+ Year Projects

*Icons for Linux, Python, GCC, Git, and C++*
Google is a leader in Open Source

- 287,024 Commits by Googlers to Open Source Projects on GitHub in 2016
- 15,000+ Projects Contributed to in 2016
- 2,500 Projects That Have Had 10+ Events from Googlers
Open Source SW

- TensorFlow
- kubernetes
- Google Cloud

HW Design Barriers to Entry

- Engineering
- IP
- Tools + Infra
- Fabrication
Curate high quality, open source hardware code

Support an ecosystem with software tools, verification and documentation

A barrier free environment for collaboration

Common Hardware for Interfaces, Processors and Systems

Linux Foundation to Host CHIPS Alliance Project to Propel Industry Innovation Through Open Source Chip and SoC Design

By The Linux Foundation | March 11, 2019

New Linux Foundation Project to Foster Flexible, Next-Generation Chip Design for Optimized Workloads

SAN FRANCISCO – March 11, 2019 – The Linux Foundation, the nonprofit organization that advances open source in the enterprise, today announced its intent to form the CHIPS Alliance project to help define open source, industry-relevant chip specifications. CHIPS Alliance will foster a collaborative environment for the creation and deployment of more efficient and flexible chip designs for use in market segments such as Internet of Things (IoT) applications.

Early CHIPS Alliance backers include Esperanto Technologies, Google, SiFive and a growing list of open source hardware and continued momentum behind the free and open RISC-V architecture.

“The RISC-V community is working to foster open source foundation technologies that help the industry move [artificial intelligence/machine learning and infrastructure composability] forward,” said Dr. Gary Wilk, vice president of IDC's Infrastructure Systems, Platforms, and Technologies Group, via statement.
CHIPS Alliance

- Many additional members in the process of joining

- Extraordinary individuals: Wilson Snyder, Olof Kindgren
CHIPS Alliance Organization

Board of Directors
- Yunsup Lee
- Zvonimir Bandic (Chair)
- Dave Ditzel
- Richard Ho (Vice-chair)
- More to be added

Interim Director
- Ted Marena

Technical Committee
- Henry Cook

Project Maintainer

Marketing
Governance Model

**Governing Board**
oversees business decisions, budgets, outreach, marketing/events, trademarks, etc.

**Technical Steering Committee**
decides on projects to be approved, top level coordination across projects

**Outreach Committee**
coordinate evangelism, communication, outreach, events, training

**Project Maintainers and Technical Team Workgroups**
deliver verified design and design verification test benches
Membership

- Like other projects of the Linux Foundation, this project is funded through membership dues and contributed engineering resources.
- Membership levels include: Platinum, Gold, Silver, Auditor, Academic.
Launch Workshop June 19, 2019

Google Sunnyvale office.
Well over 200 registered and/or waitlisted.
High energy discussions.
Lots of enthusiasm.
Examples of open source hardware and design tools contributions.

Open source RTL designs:
- Compute cores (SweRV, Rocket)
- Networks/Interfaces (OmniXtend, TileLink)

Modern design tools:
- UCB Chisel and FIRRTL
- FuseSOC (IP package manager)
- SiFive Federation: open source chip workflow
- BAG (Berkeley Analog Generator)

Addressing RTL simulation and design verification:
- Google UVM Stressful Instruction generation
- Verilator (open source Verilog simulator)
- Cocotb (Python TB) in collaboration with FOSSID
Design Verification is the Foundation of Reuse

Quality is key to reuse

- Stress testing needed to ensure IP will operate correctly when integrated into new design.
- DV accounts for >50% of project time for complex chips.
Open source RISC-V processor verification solutions

riscv-tests
A simple test framework focused on sanity testing the basic functionality of each RISC-V instruction. It’s a very good starting point to find basic implementation issues.

riscv-compliance
A suite of directed tests for RISC-V instruction groups. Includes known good signatures and allows processors to be checked for compliance to the RISC-V specifications.

riscv-torture
Scala-based RISC-V assembly generator that provides a good mix of hand-written sequences. Supports most RISC-V ISA extensions which makes it very attractive. Simple program structure and fixed privileged mode setting.

Verification is one of the key challenges of modern processor development.
Many missing pieces

- Complex branch structure
- MMU stress testing
- Exception scenarios
- Compressed instruction support
- Full privileged mode operation verification
- Coverage model
- ...

Motivation

Build a high quality open DV infrastructure that can be adopted and enhanced by DV engineers to improve the verification quality of RISC-V processors.
Google’s Stressful Transaction & Instruction Generator (STIG)

- STIG will drive your RISC-V core through corner cases and push it to the limit.
- A high quality SystemVerilog, UVM DV infrastructure:

https://github.com/google/riscv-dv
Key Features

01
Randomness
Randomize everything: instruction, ordering, program structure, privileged mode setting, exceptions..

02
Architecture Aware
The generated program should be able to hit the corner cases of the processor architectural features.

03
Performance
The instruction generator should be scalable to generate a large program in a short period of time.

04
Extendability
Easy to add new instruction sequences, custom instruction extension, custom CSR etc.
Complete feature list

- **Supported ISA**
  RV32IMC, RV64IMC

- **Supported privileged mode**
  User mode, supervisor mode, machine mode

- **Supported spec version**
  User level spec 2.20, privileged mode spec 1.10

- **Supported RTL simulator**
  VCS, Incisive, Questa, Metrics

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**Test suite**

- Basic arithmetic instruction test
- Random instruction test
- MMU stress test
- HW/SW interrupt test
- Page table exception test
- Branch/jump instruction stress test
- Interrupt/trap delegation test
- Privileged CSR test
Verification using Co-simulation with Reference Model

- **Google**: open source RISC-V-DV instruction stream generator (STIG)
- **Metrics**: SystemVerilog design + UVM simulator for RTL
- **Imperas**: model and simulation golden reference of RISC-V CPU
Summary

Open source hardware holds promise of greater innovation. Healthy, sustainable ecosystem needs industry, academia and grass-roots support.

CHIPS Alliance aims to support curated high-quality projects that are used and maintained.

Please get involved!